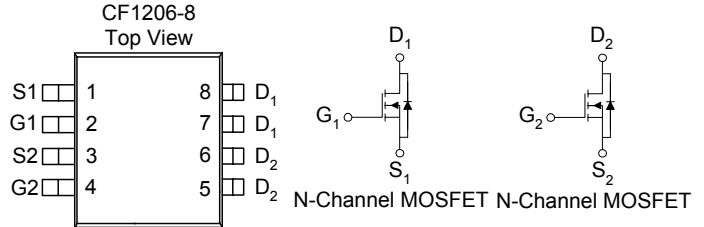


Dual N-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
20	58 @ $V_{GS} = 4.5V$	5.0
	82 @ $V_{GS} = 2.5V$	4.2

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe CF1206-8 saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current ^a	I_D	$T_A = 25^\circ C$	5.0
		$T_A = 70^\circ C$	4.1
Pulsed Drain Current ^b	I_{DM}	± 30	A
Continuous Source Current (Diode Conduction) ^a	I_S	1.7	A
Power Dissipation ^a	P_D	$T_A = 25^\circ C$	2.1
		$T_A = 70^\circ C$	1.3
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	62.5	$^\circ C/W$
	Steady State	80	$^\circ C/W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

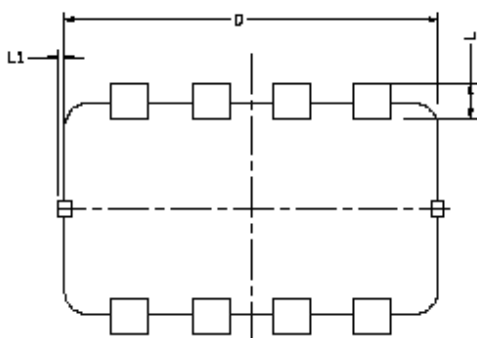
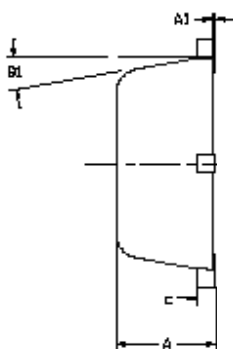
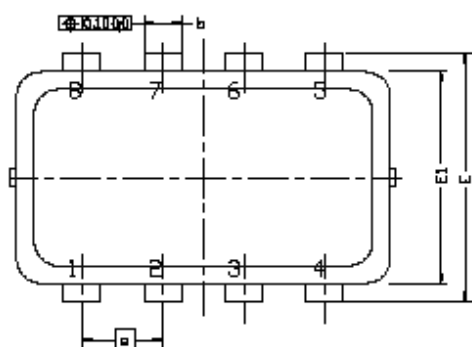
SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.7			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16 V, V _{GS} = 0 V			1	μA
		V _{DS} = 16 V, V _{GS} = 0 V, T _J = 55°C			25	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 4.5 V	20			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 5 A			58	mΩ
		V _{GS} = 2.5 V, I _D = 4.2 A			82	
Forward Transconductance ^A	g _s	V _{DS} = 15 V, I _D = 5 A		22		S
Diode Forward Voltage	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V		0.7		V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 5 A		7.5		nC
Gate-Source Charge	Q _{gs}			0.6		
Gate-Drain Charge	Q _{gd}			1.0		
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 15 Ω, I _D = 1 A, V _{GEN} = 4.5 V		22		nS
Rise Time	t _r			40		
Turn-Off Delay Time	t _{d(off)}			50		
Fall-Time	t _f			20		
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 1.7 A, di/dt = 100 A/μS		40	

Notes

- Pulse test: PW ≤ 300 μs duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

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Package Information



DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.03	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.08	0.152	0.25	0.003	0.006	0.010
D	3.00 BSC			0.118 BSC		
E	2.00 BSC			0.079 BSC		
E1	1.70 BSC			0.067 BSC		
e	0.65 BSC			0.026 BSC		
L	0.20	0.275	0.400	0.008	0.011	0.0157
L1	0	---	0.100	0	---	0.004
θ	0°	10°	12°	0°	10°	12°